February 6, 2003

A Survey of Co-Design Ideas and Technology

(draft)

by

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Chapter 1

Introduction

Due to the increasing size of integrated circuits and time-to-market requirements designing embedded systems is becoming more and more complex. This increasing complexity of embedded systems is the driving motivation for a high-level system design paradigm. A high-level system design notation could also offer substantial performance benefits as there can be a smarter partitioning of the system's parts onto hardware and software. High-level system design is currently a major research area by academics world-wide and it is strongly rooted in traditional areas such as control theory and digital design theory. For Chess such a design approach could mean a faster and better design process. This paper investigates a number of aspects of system-level design and the current state of the art in existing tools and methods that allow system-level design.

A system design paradigm should be at an abstract level that allows reasoning at a high level of abstraction. However, to be useful it must also be possible to synthesis code from this high-level language for hardware and software. How to divide the functionality of the system in hardware and software parts is a very important aspect of this synthesis. Traditionally the choice what to implement in hardware and what to implement in software is made early in the design process. Both parts are then made in separate tracks by separate design teams.

When the emphasis lies on the hardware-software partitioning problem, system-level design methods are also called "Co-Design" methods. These terms are often used mixed; in this paper we will mainly use "Co-Design."

The goal of Co-Design is to explore the whole design-space to be able to make well-informed decisions and to be able to make this decision in a later phase in the design process. This would lead to a more optimal partitioning and more flexibility during the design process. To really understand the improvement a high-level system design paradigm would be, it is important to see how traditional system design works and what the problems are with such an approach.

1.1 Traditional design

Traditionally complex embedded systems are designed around a microprocessor in a Von Neumann architecture. A Von Neumann system is fundamentally a sequential system. There is heavy optimalisation inside the CPU itself (for instance using pipelining) but ultimately the commands are executed one at a time. Systems based on microprocessors have several benefits. Microprocessors are very well optimized and they allow design of families of products that can be built. Such a family of product can provide various feature sets at a different price point and can be extended to keep up with rapidly changing markets[44].

However, the fact that each command is executed sequentially leads to a fundamental limitation. Backus [1978] calls this the "von Neumann bottleneck". He points out that this bottleneck is not only a physical limitation, but has also been an "intellectual bottleneck" in limiting the way we think about computation and how to program.

[Guus: explain difference between hardware and software as related to concurrency.] This same aspect is a major motivation for Chess to do this investigation: how to prevent the 'paradigm-shift' that often occurs in designing systems. [Guus: this paragraph should be better. Explain more what the paradigm shift is.]

Not all embedded systems are designed around microprocessors. It is possible to design embedded chips that compute in a parallel way. ASICs (application specific integrated circuites) are specialized chips, that are used for example for [...]. They are similar to processors in the sense that they are also 'hardwired' solutions. It is very expensive to design an ASIC, and a

very slow process. Therefore, customizing an ASIC for a single application is only feasible when the project is reasonably big. In any case an ASIC can only be produced when the layout is final: it is undo-able to experiment with the layout and try several versions.

Although you'll loose the optimalizations found in microprocessors there is a huge potential gain when designing hardware that is parallel in nature because the layout of the hardware can then be tailored exactly to the functional requirements. This can be extremely profitable, especially when the problem to be solved is mainly parallel in character. ASICs are therefore often used in areas such as compression, encryption etc. which are parallel 'in nature'.

An important motivation for the rising interest in Co-Design is that there now is another type of chip that is much more flexible than ASICs.

1.2 Programmable logic

Programmable logic devices (PLDs) are computer chips that can be programmed to implement circuits requiring both combinational and sequential logic. Reconfigurable logic devices are a class of programmable logic devices which may be reprogrammed as often as desired. FPGA's are reconfigurable logic devices that are becoming very popular[8]. Three direct benefits of the reconfigurable approach can be recognized: specialization, reconfigurability and parallelism[38] [Guus: use more of Tessier on future developments [38]]. FPGA's shorten the development cycle dramatically and are much cheaper to use than ASICs. This allowed research to Co-Design to increase a lot. It also made researchers consider more fine-grained approaches.

Early approaches in Co-Design therefore started with components of high granularity, such as ASIC and microprocessors. In Co-Design methods a mixture is often used. Parts of the hardware are designed from scratch, but a microprocessor is also used. This allows the system to benefit from both the microprocessor's specialization, and for the parts of the system that benefit most of this a parallel implementations. This difference in level of granularity is an important feature to discriminate on various Co-Design approaches.

Obviously designing hardware and software for a system in an integral manner is an

extremely complex task with many aspects. There is a wide range of architectures and design methods so the hardware/software Co-Design problem is treated in many different ways.

In this thesis it is investigated what methods exists that comply with the Chess business. I'll compare them with each other. I'll also investigate the problem of the paradigm shift (or the prevention of this) when designing parallelism in a high-level language. Ideally the resulting hard- and software description should be parallel in nature where possible.

In this paper I'll give an overview of the field and indicate the open issues. I'll try to answer to question which type of language is suitable for which problem.

1.3 Outline

First we'll look at what Co-Design is and the problems it tries to solve. In Chapter 5 different types of Co-Design approaches are described, and the classifications that can be made. It turns out that the paradigms, the computational models, are very important. They are directly related to the paradigm shift. Chapter 6 describes computational models that are commonly used to model (parts of) systems.

A single paradigm approach has serious disadvantages so various hybrid models have been proposed in literature. In Chapter 7 existing projects and models will be described and analyzed using the classifications and ideas found in the first part. Per method we'll look at some case studies to get a better view of how the multi-paradigm modelling works and how well it can be applied. In Chapter 8 the pro's and contra's of the investigated heterogeneous methods will be discussed.

Chapter 2

Assignment

"To investigate various development methods and to investigate how an integrated approach of HW/SW design can improve system development at Chess."

I'll give a introduction to the field of Co-Design. I will investigate the relevance and relationships between these specification and design languages in the track from specification to implementation. I'll research to which degree existing development and implementation methods support compatible paradigms.

The focus in this internship will be on the shift of paradigms when traversing through the various levels of detail.

Chapter 3

Background and related work

3.1 History

The field of Co-Design is about 10 years old now. [Guus: about Gupta paper etc]

A survery In 1998 a paper was published that described a method to synthesize code for both hardware and software, for a specific type of data-flow programs[13].

3.2 Related work

The SAVE project of the Linköping University in Sweden did a survey on Co-Design representation models in 1999[6]. [Guus: about other comparative papers]

3.3 Related approaches

3.3.1 Software in the loop

Some of the issues Co-Design tries to solve are also handled by 'Software-In-The-Loop'. This is developing software in a virtual hardware environment. Although this easies the design of software for hardware it does not allow the full improvements made possible by Co-Design.

3.3.2 Reconfigurable hardware

Reconfigurable systems exploit FPGA technology, so that they can be personalized after manufacturing to fit a specific application.

"A promise of reconfigurable hardware is that it should allow the logic and memory resources in a chip to be used more efficiently, especially in applications that need massive computing power. But there is a further commercial advantage. It could turn finished products into a source of service revenue. Imagine a music player that includes programmable logic. When a new music-compression format emerges to replace MP3, owners of the player could download, for a fee, a new decompression algorithm for their player from the maker's website"[39].

The operation of reconfigurable systems can either involve a configuration phase followed by an execution phase or have concurrent (partial) configuration and execution.[30]. The major Co-Design problem in this type of systems consists of identifying the critical segments of the software programs and compiling them efficiently to run on the programmable hardware. This is a different field and will not be treated in this thesis.

3.3.3 Adaptive computing

The field of adaptive computation is closely related to reconfigurable hardware. According to Neema the primary challenge of the Adaptive Computing approach is in system design[32].

3.3.4 Hybrid systems

Most traditional Co-Design methods explore ways of modelling digital systems. Embedded systems however, often interact with an analog environment. Traditionally, this is the domain of control theory and related engineering principles. Because of the way models are often treated (digital) the analog environment is often abstracted away (to a digital translation) by computer scientists. This way traditional Co-Design is unable to guarantee safety and/or performance of the embedded device as a whole.

To address this issue **hybrid** embedded system models have been designed[1, 37]. The issues that Co-Design faces, such as combining various models of computations and making sure properties are valid throughout the whole design phase, can of course also be found in this hybrid system modelling. In fact, the difference between the two is not always very sharp. [TBD: on

differential equations].

Chapter 4

Co-Design

Co- Design is "A design methodology supporting the concurrent development of hardware and software in order to achieve system functionality and performance goals. In particular, Co-Design often refers to design activities prior to the partitioning into Hardware and Software and the activity of design partitioning itself."[43].

4.1 Abstraction

A goal of all design methods is to allow systems to be designed on a higher level than the implementation level. The ultimate goal is to allow a very high-level design, that then automatically can be converted into the implementation level. This is a fundamental notion in computer science. Examples are programming languages, that allow humans to reason about variables or flow-of-control on an much higher level than machine code allows. Analog have there has been a lot of research into finding languages to design hardware from a higher level. Nowadays it is very common to use a language as VHDL to define hardware. There are compilers available to generate netlists (hardware descriptions) languages like VHDL. Although VHDL is considered for software engineers to be low-level, it is a major step forward compared to the arcane art of programma cells and gates directly.

This looking for a higher level of abstraction is an ongoing quest, and as so it can also be found in Co-Design methods. Ultimately the goal is to be able to design a system in a textual or graphical way, in such a manner that there will be an automatic compiler from this high-level

representation into the implementation level: hardware, software or (often) a combination of both. Sometimes such an approach is called model compilation[35].

4.2 Modelling and specification

Modelling is the process of conceptualizing and refining the specification. The result of the modelling phase is a model, which is specified in a internal design representation. There are several tasks that must be performed to create a system-level design model. To comprehend the benefits of various Co-Design technologies it is important to understand how the design process works.

The Co-Design system design process for embedded systems includes modelling, validation, and implementation[30]. These processes are fundamental steps in any methodology aimed to design an embedded system.

'There is a subtle relationship between the specification of a system and the modelling of a system. An executable specification, for example, is also a model of an implementation. The difference is in emphasis. A specification describes the functionality of a system, and may also describe one or more implementations. A model of a system describes the functionality. In a specification it is important to avoid over-specifying the design, to leave implementation options open. In a model, often the key criteria are precision, simplicity and efficient simulation. A model should be the most abstract model that represents the details being tested.'[5].

Specification is closer to the problem level, at a higher level of abstraction, and uses one or more models of computation. A specification undergoes a synthesis process (which may be partly manual) that generates a model of an implementation. That model itself may contain multiple models of computation.

The outcome of the modelling process is the internal design representation (IDR). There is a trade-off between scalability and expressiveness in this IDR[42]. In Chapter 5 we'll go deeper into the modelling process.

4.3 Validation

Through the validation process, the designer achieves a reasonable level of confidence about how much of the original embedded system design will be in fact be reflected in the final implementation.[42]. There are 3 three methods for validation:

(1) Simulation

(2) Prototyping

(3) Formal Verification

There has been a lot of research in the simulation of heterogeneous hardware/software systems [42, 22, 5]. Formal verification allows for a more thorough test of the embedded system behavior (maximum behavioral coverage) by means of logics.

4.4 Synthesis

The final stage in the development of an embedded system is the synthesis process. It is an important notion in a Co-Design approach that there is no continuity problem. That is: the steps from model to the synthesis should be all in the design process[35].

In the phase architectural information is taken into account. Varea[42] calls this a merger between the IDR with the **technology library**. It is important that the intermediate IDR or specification is not too operational (influenced by the current technology), it will bias the design towards a specific architecture.

4.4.1 Hardware/software Partitioning

[Guus: should be somewhere else]. 'The partition of a system into hardware and software is of critical importance because it has a huge impact on the cost/performance characteristics of the final design. In the case of embedded systems, a hardware/software partition represents a physical partition of system functionality into application-specific hardware and software executing on one (or more) processor(s).'[30]. When considering general purpose computing systems,

a partition represents a logical division of system functionality, where the underlying hardware is designed to support the software implementation of the complete system functionality. This division is elegantly captured by the instruction set. Thus instruction selection strongly affects the system hardware/software organization.

Obviously is important to look at the architectural organization of the system. Although it is possible to generate a complete system using only FPGA's, it is very common to use a combination of 1 (or more) processors with dedicated hardware. This is called **coprocessing**[30]

On the lowest level, FPGA's can be used to implement SM's, datapaths and nearly any digital circuit. The outcome of the synthesis process is a final implementation of the embedded system.

Chapter 5

System Level Modelling

Approaches to hardware/software Co-Design of embedded systems can be differentiated in several ways. One way is to consider the system-level specification, which is either homogeneous (i.e., in a single specification language) or heterogeneous (i.,e. involving multiple modelling paradigms)[31]. Another way is to distinguish how the design methods deal with the SW/HW partitioning: fine-grained or coarse-grained. Modelling in the context of Co-Design is sometimes called **cospecification**.

5.1 Homogenous modelling

Homogeneous modelling implies the use of single specification language for the modelling of the overall system. Lee[23] calls this the 'grand unified method'. Co-design starts with a global specification given in a single language. This specification may be independent of the future implementation and the partitioning of the system into hardware and software parts. In this case Co-Design includes a partitioning step aimed to split this initial model into hardware and software. The outcome is an architecture made of hardware processors and software processors. The is generally called a virtual prototype and may be given in a single language or different languages[19]. Lee sees as a big problem that a homogenous approach imposes a model of computation which might be good for a subset of systems but bad for others[23].

5.2 Heterogeneous modelling

Heterogeneous modelling allows the use of separate languages for the hardware and software parts. The Co-Design starts with a virtual prototype where the hardware/software partitioning is already made. Here the emphasis is on the integral designing of the parts to make sure the overall system has the required properties. The key issues are validation and interfacing [19]. A lot of research is done on the integration of different system parts tat enables system optimization across language boundaries. [this sentence from the SPI Workbench].

5.2.1 Co-simulation vs. compositioning

[7] differences between 2 different types of heterogenous modelling. The compositional approach aims at integrating the partial specification of sub-systems into a unified representation which is used for the verification and design of the global behavior. Examples are Polis, Javatime and SpecC.

The cosimulation-based approach consists in interconnecting the design environments associated to each of the partial specifications. Like its names suggests, with co-simulation the software parts and the hardware components of an system and their interactions are simulated in one simulation. It does not provide such a deep integration as compositioning does however it does allow for modular design. Communication is often done using a cosimulation bus, that is in charge of transferring data between the different simulators.

The Cosimulation-field is reasonably well established. Sometimes cosimulation is used to simulate the behavior of a system consisting of 2 models: the hardware and the software, and sometime it is used to model on a more abstract level where the hardware vs software decision has not been made yet. [Guus: really? This is interesting. Expand on this.]

It is good to note that the hardware is often simulated (although often not real-time, as it's just a simulation). However there has also been some research in replacing the hardware simulator with an FPGA (or multiple FPGAs) that simulate the real target hardware[22].

It is clear that the choice of an IDR is a very important aspect of a Co-Design method, therefore in the next chapter we'll go into the various types of IDR's there are.

Chapter 6

Computational Models

Modelling is a the heart of development methods. The computational models can be found in the Immediate Representation Language. All Co-Design systems are based on a computational model, or combine a few of them.

A computational model is a formal, abstract definition of a computer. It describes the components in a system and how they communicate and execute. Several models exists. There are a number of authors who made an overview of various development methods, i.e. [45], [19].

[Guus: here explain what I want to find about of the models]. Ie, timing, hierarchy.] An essential difference between concurrent models of computation is their modelling of time. [23] (page 11). Lui[25] states that the different notions of time make programming of embedded systems significantly different from programming in desktop, enterprise or Internet applications. Lee[24] proposed a mathematical framework to compare certain properties of models of computation. This allows for a precise definition of the various computational models.

In the Chapter a few 'basic' Models of Computations are described.

6.1 Concurreny or: Dataflow vs. Control flow oriented

[Guus: insert examples here]. Fundamental to embedded software is the notion of concurrency. There is a lot of research done on compiling concurrent languages into sequential code that can be run on a microprocessor, see for example [20]. For this thesis however it is more interesting to see what happens when this paradigm-shift does not have to be made.

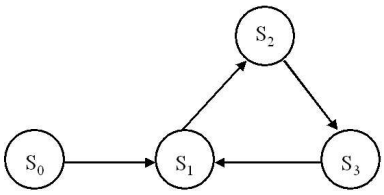


Figure 6.1: A state transition graph.

There are models that are designed to describe dataflow oriented systems (ie DSPs) and there are models more suitable for control-flow systems.However this approach lacks generality as most systems are not easily put in either one category. It should be noted that the difference between a control-flow or data-flow oriented computational model is important for both control and data-oriented systems. Many control-systems use complex sensors or subsystems such as image processing algorithms that are best specified using a type of data-oriented computational model[26].

6.2 Common computational models

6.2.1 Finite-state machines

The finite-state machine model has been widely used in control theory and is the foundation for the development of several models for control-dominated embedded systems. The classical FSM consists of a set of states, a set of inputs, a set of outputs, a function which defines the outputs in terms of input and states and a next-state function.[6].

FSMs model systems where the system at any given point in time can exist in one of finitely many unique states. This makes them excellent for control logic in embedded systems. They can very well be formally analyzed and it is relatively straightforward to synthesis code from this model[23].

FSM can be visualized very well using a state transition graph (see Figure 6.2.1). FSM have a number of weaknesses. They are not very expressive, and the number of states can get very large even in the face of only modest complexity. Is intended for control-oriented

systems with relatively low algorithmic complexity. A number of variations has been proposed to overcome to weaknesses of the classical FSM model. Using FSMs in a hierarchical model was first made popluar by Harel[26]. He proposed StateCharts, which combine heriearchical FSMs and concurrency. In Chapter 7.7 we'll see some examples of heteregenous models based -partly- on FSMs.

6.2.2 Imperative models

In an imperative model of computation, modules are executed sequentially to accomplish a task. This is the most trivial computational model there is and most authors don't even mention it. However in Chang's paper[5] it is mentioned because it can be used in combination with other models in a hierarchical system. See also Chapter 8.1.

6.2.3 Differential Equations

These are often used to model mechanical dynamics, analog circuits, chemical processes and many other physical systems. [14].TBD. When using real numbers as time model, continuous-time systems are active over the entire time axis processing their input and producing output.[37].

6.2.4 Difference Equations

Like differential equations, but discrete. TBD. These two are very important as they deal with a very common type of signal from the outside world. Discrete-time systems can only react to their input and produce new output at distinct, equidistant time instances. [37]

6.2.5 Process networks and dataflow

In a process network model of computation the arcs represent sequences of data values (token) and the bubbles represent functions that map input sequences into output sequences. Certain technical restriction are necessary to ensure determinacy.[23]. It is a common represen-

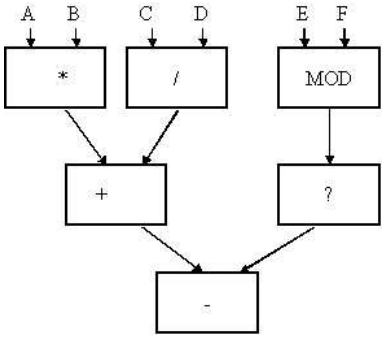


Figure 6.2: Dataflow for (A * B) + (C/d) - (sqrroot(e mod f))

tation formalism for modeling algorithms. The graph representation can be interpreted asynchronous (ADF) or synchronous (SDF). [Guus: uitwerken wat voor soort data-flow modellen er allemaal bestaan.]

6.2.6 Discrete-event models

In a discrete-event system, modules react to event that occurs at a given time instant and produce other events either at the same time instant or at some future time instant. Execution is chronological[5]; time is an integral part of the model. Events will typically carry a time stamp, which is an indicator of the time at which the event occurs within the model. A simulator for Discrete-Event models will typically maintain a global event queue that sorts events by time stamp. This sorting can be computationally costly. [Guus: hard to simulate, nice in hardware].

6.2.7 Petri Nets

In the classical approach a Petri net is composed of 4 basic elements: a set of places, a set of transition, an input function that maps transitions to places, and an output function which is also a mapping from transition to places. This is an well-understood modelling tool. Two important features of Petri nets are its concurrency and asynchronous nature.[6]. [Guus: expand a little bit: where are petri nets good for?]

6.2.8 Synchronous models

In synchronous languages, modules simultaneously react to a set of input events and instantaneously produce output events. If cyclic dependencies are allowed, then execution involves finding a fixed point, or a consistent value for all events at a given time instant.[5]

Very often real-time systems are specified by means of concurrent processes, which communicate asynchronously [34].

The synchrony hypothesis forms the base for the family of synchronous languages. It assumes, that the outputs of a systems are synchronized with the system inputs, while the reaction of the system takes no observable time. So time is abstracted away. The synchrony hypothesis abstracts from physical time and serves as a base of a mathematical formalism. All synchronous languages are defined formally and system models are deterministic.

'In synchronous languages, every signal is conceptually (or explicitly) accompanied by a clock signal. The clock signal has meaning relative to other clock signals. It defines the global ordering or events. Thus, when compariung two signals, the associated clock signals indicate which events are simultaneous and which precede or follow others. A clock calculus allows a compiler to reason about these ordering relationships and to detect inconsistencies in the definition.'[5].

This model serves as a good implementation model.

6.2.9 Rendezvous models

In a rendezvous model, the arcs represent sequences of atomic exchanges of data between sequential processes, and the bubbles presents the processes. [23]. Examples are Hoare's CSP and Milner's CCS. This model of computation has been realized in a number of concurrent languages, like Lotos and Occam. [Guus: based on algebra? How is timing handled?]

6.3 Comparison

[6] also made a comparison of various computational models.

Computational model	Timing	Property X
Differential Equations	?	?
Difference Equations	?	?
SDF	No explicit timing	Synchronous
ADF	No explicit timing	Asynchronous
Discrete-event models	Globally sorted events with time tag	?
Petri Nets	No explicit timing. Just order of transitions[6]	Asynchronous
Synchronous/reactive models	No explicit timing	Synchronous
Rendez-vous	Atomic events along line of time[6]	Asynchronous

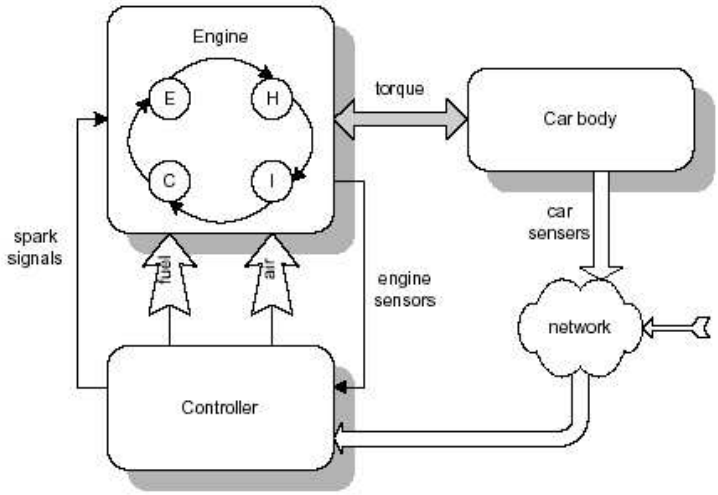
Chapter 7

Heterogeneous systems

Heterogeneous systems are systems that allow more than one computational model in a system to be used. Experience suggest that several MoC are required for the design of a complete system.[5]. A nice illustration of the need for multiple computational models can be found in [25]:

[Guus: how can you determine system behaviour for these types of systems? Things like deadlocks, lifelock, timing...]

7.1 Example: internal combustion engine



A cylinder of an internal combustion engine has four working phases: intake, compress, explode, and exhaust. The engine generates torque that drives the power train and the car body.

Depending on the car body dynamics, the fuel and air supply, and the spark signal timing, the engine works at different speeds, and thus makes phase transitions at various time transitions. The job of the engine controller is to control the fuel and air supplies as well as the spark signal timing, corresponding to the drivers demand and available sensor information from the engine and the car body.

The engine and the car body in this example are mechanical systems, which are naturally modelled using differential equations. The four phases of the engine can be modelled as a finite state machine, with a more detailed continuous dynamics for the engine in each of the phases. While all the mechanical parts interact in a continuous-time style, the embedded controller,. which may be implemented by some hardware and software, works discretely.

Additionally, sensor information and driver's demands may arrive through some kind of network. The controller receives this information, computers the control law, controls the air and fuel values, and produces spark signals, discretely. So, we want to use a model that is suitable for handling discrete events for the network and the controller.

In this very common example, we have seen both continuous-time models and several discrete models: finite state-machines, discrete events, and real-time scheduling.

It's common for a specification language to allow more than 1 model of computation. However this does not always mean that this allows for suitable high-level mixture of 2 models. An imperative language can be used to implement for example a dataflow MoC[5]. It is obvious that low-level languages such as VHDL are able to implement different models of computation. However, their lack of abstraction disqualifies them as candidates for modelling combined computational model-systems because it leaves programmers no freedom to make trade-offs between programmability, utilization of resources and silicon area.

7.2 Old tools revived

Many languages and tools that were developed based on a single model start to embrace other models [14]. The downside of such large languages with multiple MoC's is (according

to [5]) that formal analysis may become very difficult. It compromises the ability to generate efficient implementations or simulations and makes it more difficult to ensure that a design is correct. It precludes such formal verification techniques as reachability analysis, safety analysis and liveness analysis.

Most complex system are a combination of data- and control-flow oriented parts. Varea[42] proposes a classification according to the following taxonomy:

(1) Models originally developed for control-dominated embedded systems and later expanded to include data-flow (these models will be called $\mathcal{M}_{CD}$).

(2) Models developed in a data-dominated basis extended to support also control flow (referred to as $\mathcal{M}_{DC}$

(3) Unbiased model developed specifically to deal with combined control/data-flow interactions ($\mathcal{M}_{\bar{b}}$)

[Guus: use this classification!]

As noticed in Chapter 3.3.4 the modelling of hybrid digital-analog systems is a related field that is gaining more attention too. Also in this field there are existing tools that are extended with functionality to deal with hybrid modelling. Examples of this are VHDL-AMS.

7.3 New heterogeneous tools

However also new frameworks have been developed that took multiple models of computations into their design from the beginning. A framework is a software architecture that specifies the possible interactions of componenets, provides a set of services that components can use and may have a set of formal properties for the system.

In this Chapter we'll see a few of the most famous modelling methods and a few that have been selecting because they are special. [Yes, this should be a different sentence].

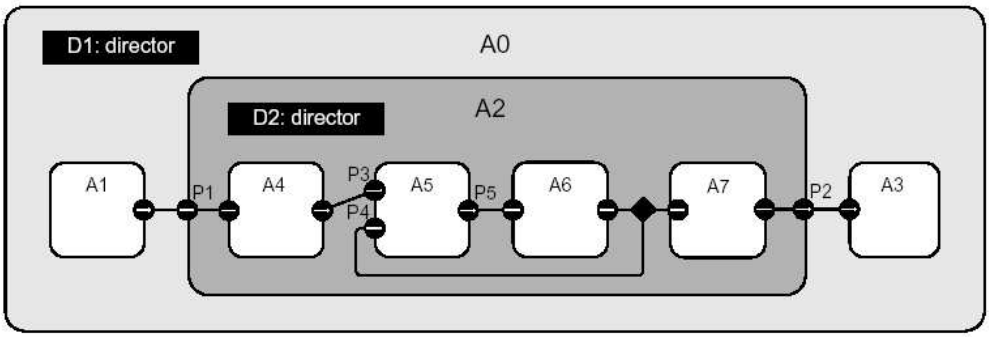
7.4 Ptolemy II

The Ptolemy project studies heterogeneous modelling, simulation and design of concurrent systems, where the focus is on embedded systems.[10].

The primary investigator of the Ptolemy project is Edward A. Lee. In 1991 he presented a paper[4] that described the Ptolemy system. This system has been in use for many years, and it's now succeeded by a new version, Ptolemy II.

The Ptolemy II software environment provides support for hierarchically combining a large variety of models of computation and allows hierarchical nesting of models.[14]. It combines the wish for a homogeneous and thus predictable model with the desire to mix partial models of different kinds in a common heterogeneous model by hierarchically nesting sub-models of potentially different kinds.

A very good description of how this hierarchical mixed approach works in practice can be found in [26].



Ptolemy II is a component-based design methodology. The components in the model are called actors. A model is a hierarhcial compostition of actors. The ataomic actors, such as A1, only appear at eh bottom of the hierarchy. Actors that contain other actors, such as A2, are composite. A composite actor can be contained by another composite actor.

Atomic actors contain basic computation, from as simple as an AND gate to more complex

as aan FFT. Through composition, actors that perform even more complex functions can be built. Actors have ports, which are their communication interfaces. For example in the figue, A5 receives data from input ports P3 and P4, performs its computation, and sends the result to output port P5. A port can be both an input and an output. Communication channels among actors are established by connecting ports.

The possibility to have various MoC's can be found in the **director**. A director controls the execution order of the actors in a composite, and mediates their communication. In figure 1, D1 may choose to execuyte A1, A2 and A3 sequentially. Whenever A2 is executed, D2 takes over and executes A4-A7 ascoordingly. A direcor uses receivers to mediate actor communication. As shown in figure 2, one receiver is created for each communication channel; it is situated at the input ports, although this makes little difference. When the produces actors sneds a piece of data (a token) to the ouput port, the receiver decise how the transaction is completed. Within a composte actor, the actors under the immediate control of a director interact homoheneously.

7.5 COSYMA

A bit older design method is COSYMA, "CoSynthesis for Embedded Architectures". It was developed at the IDA, Germany. It covers the entire design flow, from specification, to synthesis. The target architecture consists of a standard RISC processor, a fast RAM for program and data with single clock cycle acceess time and an automatically generated application specific co-processors. Communication between processors and co-processor takes place through shared memory.

The system is designed in Cx. This is a C-extension with support for parallel processes and timing constraints. The Cx specification is then converted into an Extended Syntax Graph (ESG), the IDR. The ESG describes a sequence of declarations, definitions and statements and is overlayed with the Data Flow Graph (DFG) containing information about data dependencies.

Research using COSYMA has been discontinued in 1999.

7.6 Simulink

Existing (commercial) tool. [25] calls it a framework. A modelling and simulation environment for continuous-time dynamic systems with discrete events. It has been extended with StateFlow[26].

7.7 *charts

Statecharts are essentially a combination of FSMs with a SR. The tools Statemate from Ilogix uses statecharts as its control specification model.

A recent development is *Charts (pronounced Starcharts). TBD

[Guus: SOLAR here[7]]. Another model based on Finite State Machinbes is the CFSM model. The communication primitive is called event.[6].

7.8 ForSyDe

An interesting method has been development by Sander and Jantsch[33, 34]. In their model events are totally-ordered by their tags. Every signal has the same set of tags. Events with the same tag are processed synchronously. There is a special value $\perp$ ("bottom") to indicate the absence of an event. These are necessary to establish a total ordering among events. A system is modelled by means of concurrent processes; it is a model based on the synchronous-assumption (see Chapter 6.2.8).

Lu[27] shows how to transform a system specification described in ForSyDe into its hardware and software counterparts. He does not provide a mixed implementation of HW and SW. [Guus: why not per module possible to make this decision?]

The hardware version of the Digital Equalizer that Lu makes is described using behavioral VHDL. The process are described using skeletons and these are then synthesized to VHDL code. The process described is manual. The Haskell code turns into behavioral VHDL quite easily. To generate (naturally sequential) C code an analysis phase is done to create a PASS.

[3] also investigated the design of a Digital Equalizer. They used a combination of SDL and Matlab as their design languages.

SDL is used to model the control parts, Matlab is used for the DSP parts.

7.9 Moses framework

7.10 Solar/Music

[7] describes a multi-language approach at the system level providing both system-level refinement and high-level interfaces synthesis.

7.11 FunState/SPI Workbench

FunState is an internal design model based on functions driven by state machines[40]. It is an enhancement of the older SPI Workbench[46].

The SPI Workbench [46] is based on intervals of system properties and is specifically targeted to cosynthesis. Made for performance estimations. [Guus: Funstate = new version of SPI workbench?]

7.12 Metropolis

7.13 IRSYD

IRSYD[15] is an acronym that stands for Internal Representation for System Description. It is thus an internal design representation language; not a complete method. However IRSYD is fully defined and implemented (in C++).

It is quite ambitious in the sense that it claims to be able to be used for synthesis, performance estimation, formal verification etc.

The basic idea in IRSYD is a unified graph representation for control flow and data flow. It is a Flow Chart extended to handle hierarchy, both structural and behavioral, different

data types and different communication mechanisms. A flow chart is an informal graphical description of an algorithm built as a directed graph.

Unfortunately the work on this representation seems to have stopped. The latest papers are from 1998. One of the authors of some papers about IRSYD, Axel Jantsch, is also working on ForSyDe.

7.14 Comparison

Model	MoC based on	Main application
Ptolemy II	Multiple MoC's	
COSYMA		
SimuLink		
charts		
ForSyDe		
FunState	FSM with functions	
Metropolis		
IRSYD	Flow Charts	

Chapter 8

Discussion of hybrid models

Many parts in the design of embedded system require manual decisions, this remains so when using Co-Design methods. The integration Co-Design offers is valuable because of validation and easier synthesis of code from a model that allows hard- and software to be generated.

Because of the complexity of most systems, optimal manual decisions are sometimes not feasible. There are simply to many possibilities to consider. To use all of to potential improvements that a later HW/SW partition decision allows, it is therefore very important to reduce the user-decisions as far as possible. This has been recognized an there are various methods for systematic design space exploration cite(cassidy). "In order to perform rigorous analysis and synthesis it is essential to prunte the design space retaining only the most viable alternatives." In the past heuristics have been used to prune large design spaces. However, due to the complex behavior and interactions in multi-mdal systems it is difficult to come up with effective heursitcs. A better approach is to use constraints to explore and prune the design spaces; constraint satisfaction can elimante the deisgns that do not meet the constraints. The pruned design specae contaisn only the designs that are correct with respect to the appliec constraint. These desings can then be simulated, synthesized an tested."[32].

8.1 Hierarchy/Emergent behavior

'Brute-force composition of heterogeneous models may cause emergent behavior. Model behavior is emergent if it is caused by the interaction between characteristics of different formal models and was not intended by the model designer.'[14]

A common way to prevent unwanted emergent behavior is isolating various subcomponents and letting these subcomponents work together in a hierarchical way. Hierarchical in the sense of a containment relation, where an aggregation of components can be treated as a (composite) component at a higher level. In general, hierarchies help manage the complexity of a model by information hiding – to make the aggregation details invisible from the outside and thus a model can be more modularized and understandable[25].

'Note that in Ptolemy, models of computations are mixed hierarchically. This means that two MoC's do no interacts as peers. Instead, a foreign MoC may appear inside a process. In the old version of Ptolemy, such was process is called a wormhole. It encapsulates as subsystem specified using one MoC within a system specified using another. The wormhole must obey the semantics of the outer MoC at its boundaries and the semantics of the inner MoC internally. Information hiding insulates the outer MoC from the inner one.' [5]. This approached of wormholes was a bit biased towards data-flow computational models. In Ptolemy II it was replaced with opaque composite actors[10].

There are other ways to mix models of computation too. Statemate uses views. [Guus: are these views related to what Jantsch[18] calls analytical slicing into domains?]

8.2 On synthesizing code

A discrete-event model of computation is well suited for generating hardware. It is not very suitable to generate (sequential) software[5] (p. 131). 'This is for example why VHDL simulate the the designer by taking so long. A model that heavily uses entities communicating through signals will burden the discrete-event scheduler and bog down the simulation. Thus, a

specification built on discrete-event semantics is a poor match for implementation is software.

By contrast, VHDL that is written as sequential code runs relatively quickly but may not translate well into hardware. The same goes for C: it runs very quickly and is well suited for software, but not for specifying hardware. [Guus: Expand this. What are the problems with C?]

It is possible to conclude that the two issues found in this paper are closely related. If you want a single specification language you'll loose in the paradigm-shift. It is hard to imagine an (efficient) language that allows both control- and dataflow types to be presented and generate efficient code for it for all types of applications. On the other hand, if you don't mind taking the HW/SW decision earlier there are very good integrated tools and frameworks that allow working with both parts of your system in a systematic way. Code generation (or hardware generation) is easier in this style.

[21] also realizes this. He says: "the refinement approach has proven to be very effective for implementing a single algorithm into hardware. The approach is, however, less effective for a set of applications. In general, the refinement approach lacks the ability to deal effectively with making trade-offs in favor of the set of applications."

There is also a mixed form possible. This mixed form would not be applicable for every type of system, but only for a subset. An example of such an approach is ForSyDe. They allow the specification of both control- and dataflow parts in a single language. They have shown to be able to generate (reasonably) efficient code. A thing to investigate would be for what types of systems this kind of Co-Design approaches are suitable, and for which not.

Dataflow and finite-state models of computation have been shown to be reasonably re-targettable. Hierarchical FSMs such as Statecharts can be used effectively to design hardware or software. It has also be shown that a single dataflow specification can be partitioned for combined hardware and software implementation.'[5] [Guus: very interesting, expand this].

The difference made between heterogeneous and homogenous modelling seems to be a bit to blunt. Some authors make it look like heterogenous modelling is the only answer possible

because that's the only type of method that allows all kinds of systems to be modelled. However, some homogenous modelling tools allow for a subset of applications to be modelled. This way –for specific applications– the benefits of having a single language will be available without a drawback in the paradigm-shift. This relates to the conventional wisdom that high performance while minimizing resources needed (or time needed) can be obtained by matching the architecture to the algorithm[32].

The main difference in the two approaches in my view is that the true heterogenous style (like Ptolemy II) allow for more types of MoC's, and are better capable of working with new MoC's. The other option promises a closer integration though.

8.3 Paradigm shift

It has been recognized in literature that there is an important relationship between the model of computation and the target-architecture. Kienhuis et all.[21] speak in this context about a mapping between a model of computation and the architecture: "In mapping we say that a natural fit exist if the model of computation used to specify applications matches the model of architecture used to specify architectures and that the data types used in both models are similar."

Algebraic formal methods are not capable of dealing with the complexity of complete (embedded) systems design technologies. The algebra is not sophisticated enough and the design technologies are not suited toward formal verification. For the description of MoC's[24] and the interactions between them formal methods have been very valuable.

Chapter 9

Conclusions

A synergistic approach of hardware and software and taking design to higher level are nowadays recognized as mandatory to keep up with the increasing complexity of embedded systems design.

Most Co-Design tools make use of an internal representation for the refinement of the input specification and architectures[19]. Many such internal representations exist. They are all based on one or more Computational Models.

Experiments with system specification languages have shown that there is not a unique universal specification language to support the whole design process for all kinds of applications. [19].

The fundamental computation model to use is first of all dependent on the type of problem to be solved. However there is a definite trend towards heterogenous modelling systems that allow more mixed types of systems to be modelled.

Many researchers are doubting whether a grand unified approach will work. Specifically the group of Edward A. Lee (who created the Ptolemy system) has doubt about this[5]. In order to be sufficiently rich to encompass the varied semantic models of the competing approaches, they become unwieldy, too complex for formal analysis and high quality synthesis. He claims that generality can be achieved through heterogeneity, where more than model of computation is used.

Ptolemy II seems to be the most mature of the tools investigate, specifically the theoretical

foundation of mixing various computational models is well thought-out.

[Guus: etc etc... this will take a lot of work!]

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